COMPLEMENTARY TWO TRANSISTOR ROM CELL

Abstract of the Disclosure

A method and structure for a read only memory (ROM) cell array has the first drain of a first transistor connected to a true bitline and a second drain of a second transistor connected to a complement bitline. The first transistor also includes a first source, and the second transistor includes a second source. The connection of the first source or the second source to ground programs the ROM cell. With the invention, only the first source or the second source is connected to the ground and the other is insulated from electrical connections. Further, the connection of the source to ground comprises an electrical connection formed during manufacturing of the first transistor and the second transistor.

Figures